At section 4 of the office action, claims 1-31 are rejected under 35 U.S.C. 102(e) as being anticipated by *Moro* (U.S. Publication No. 2003/0056050) in view of *Iida et al.* (U.S. Patent No. 2004/01566242, hereafter referred to as *Iida*). The Examiner states that *Moro* discloses a method for enhancing performance of a memory card by operating SPI or SD-1 mode so that there are N-M unused data lines, and generating a further signal so as to cause data to be exchanged using at least one of the unused data lines (Figure 6, paragraphs 0055-0059, Figure 6). The Examiner admits that *Moro* does not specifically disclose the step of causing the exchange of data between the host module and the memory device using at least one of the unused data lines, but points to *Iida* for disclosing such data exchange (figure 2, table 2, paragraphs 0041-0045).

It is respectfully submitted that *Moro* discloses using one host device to exchange data with two SD cards.

Paragraph 0056 describes the use of DAT0 to DAT4 in different modes as shown in Figure 5. As can be seen from Figure 5, *Moro* discloses three different modes: SD 4-bit mode, SD 1-bit mode and SPI mode.

In paragraph 0056, *Moro* discloses that when SD 4-bit mode is used, all four data lines DAT3 to DAT0 are used for transferring data. No unused data lines are available. Thus, this mode has nothing to do with the claimed invention. When SD 1-bit mode is selected, only DAT0 is used for data transfer. DAT1 and DAT2 are not used. DAT3 may be used for asynchronous interruption. However, no data is exchanged on the unused DAT1 or DAT2 lines. When SPI mode is used, only DAT0 is used for data transfer. DAT1 and DAT2 are not used. DAT3 is used for transmission of chip-set select. Again, no data is exchanged through DAT1 or DAT2.

In paragraph 0057, *Moro* describes using one host device to exchange data with two SD cards in the SD mode as shown in Figure 6. In paragraph 0058, *Moro* describes using one host device to exchange data with two SD cards in the SPI mode. These paragraphs are irrelevant to the claimed invention.

In paragraph 0059, *Moro* describes a lead-through current prevention function as illustrated in the flow-chart (Figure 8). This current prevention function is irrelevant to the present invention.

In sum, *Moro* does not disclose "causing an exchange of data, using at least one of the unused data lines" even in SD 1-bit mode. *Moro* does not disclose using any unused data lines for data transfer based on at least one further signal as admitted by the Examiner.

In contrast, in the claimed invention, data is caused to exchange on at least one of the unused data line due to the generation of at least one further signal when the host module is operated in the data mode that has unused data lines.

Iida discloses a method of bus width switching for data transfer in a card type storage device. In the card type storage device, the data terminals are provided with pull-up resistors and the data terminals are connected to a level detection circuit. The detection circuit is used to detect whether one or more of the pull-up resistors are in the open condition so as to determine the bus width for data transfer (paragraph 0009). Thus, while *Iida* discloses a mode selection procedure where one of the conventional MMC mode, 1-bit high speed MMC mode, 4-bit high speed MMC mode and 8-bit high speed mode is selected for data transfer, *Iida* does not disclose the step of causing the exchange of data between the host module and the memory device using at least one of the unused data lines.

Furthermore, what *Moro* is trying to do is to prevent the use of unused data lines by using "the lead-through prevention function" (paragraphs 0043, 0045, 0051, 0052). The purpose of *Moro's* invention is to prevent a flow of lead-through current via unused data lines in order to obtain higher safety and less power consumption (paragraph 0009, 0010). In *Iida*, there is no other data transmission between a card and a host than the data transmission defined by the selected mode. There is no incentive to combine the teachings of *Moro* and *Iida* regarding the usage of the unused data lines.

For the above reasons, *Moro* in view of *Iida* does not render the claimed invention obvious.

CONCLUSION

Claims 1-31 are allowable over the cited *Moro* and *Iida* references. Early allowance of all pending claims is earnestly solicited.

Respectfully submitted,

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